[redacted]

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD, ET AL., Defendants.	Case No. 2:22-cv-293-JRG (Lead Case) JURY TRIAL DEMANDED [redacted]
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-cv-294-JRG (Member Case) JURY TRIAL DEMANDED [redacted]

MICRON DEFENDANTS' REPLY IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF LACK OF WRITTEN DESCRIPTION FOR U.S. PATENT NO. 11,093,417 (DKT. NO. 370)

[redacted]

TABLE OF CONTENTS

[redacted]

TABLE OF AUTHORITIES

Page(s)

Cases

[redacted]

TABLE OF EXHIBITS

Ex. No.	Description
A	Exhibit C to Opening Expert Report of Dr. Mangione-Smith
B	*Netlist Inc.*, v. *Samsung Electronics Co., Ltd., et al., Markman* Hearing on September 26, 2023
C	Redline comparison of the text of the ’417 patent and its parent U.S. Patent No. 10,89,314
D	Exhibit B to Rebuttal Expert Report of Dr. Mangione-Smith
E	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)
F	Excerpt from the deposition transcript of Peter Gillingham, taken on January 11, 2024

[redacted]

I. INTRODUCTION

Summary judgment of no written description is warranted. For the "CAS latency"[1] limitation, Netlist's argument, with respect to write commands, requires changing the Court's construction of "the time when data is ***made available to*** . . . ***the memory module***" to "the time that data is ***available from the buffers*** to the memory devices." This is not, as Netlist contends, a "classic battle of the experts"—Netlist has not identified written disclosure for the claims as construed.

Netlist's arguments for the "data buffer control signals" limitation fare no better. For that limitation, Netlist conflates disclosures of "control signals" with "data buffer control signals" but ignores that "control signals" and "data buffer control signals" are discussed and claimed as separate things. Disclosure of "control signals" does not provide adequate written description.

Accordingly, the Court should grant summary judgment for the '417 patent.

II. RESPONSE TO NETLIST'S DISPUTED MATERIAL FACTS

Netlist does not dispute UMF Nos. 1-6 and 8 with the exception of inserting additional characterizations that, as explained below, do not change the lack of written description analysis. Dkt. No. 453 at 1-3. Netlist disputes UMF 7, but only to the extent that Netlist identified language in the Abstract and Summary that parrots the CAS latency claim language at issue. *Id*. at 2.

III. ARGUMENT

A. There is No Adequate Written Description for the CAS Latency Limitation

As Micron explained, there is no written description with respect to data being written ***to*** a memory module because (i) "overall CAS latency" under the Court's construction is determined

[1] U.S. Patent No. 11,093,417 claim 1: "wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices." *See* Dkt. No. 370 at 2.

[redacted]

before the write command enters a memory module, and (ii) the specification only discusses delaying data transfers ***within*** a memory module (*i.e.*, ***after*** a write command enters a memory module). Dkt. No. 370 at 5.[2] ***After***-occurring delays (within a memory module) do not cause the "overall CAS latency of the memory module" to be "greater than" anything, much less "greater than an actual operational CAS latency of each of the memory devices" as claimed. *Id*. at 5-6. Netlist failed to respond to this argument.

Netlist instead argues incorrectly that a "classic battle of the experts" exists because its expert identified disclosure with respect to [redacted] Dkt. No. 453 at 5-6. Not so. There are two primary problems with Netlist's argument. First, the alleged disclosure relates to a "data buffer"—a discrete component that can be placed on a memory module. The Court's construction of "overall CAS latency," by contrast, requires looking at the timing with respect to the "memory module." Second, the alleged disclosure relates to when data is made available from a data buffer ***to the memory device***. *See, e.g.*, Dkt. No. 453 at 6 [redacted] The Court's construction, by contrast, requires looking at when data is made available either (i) ***to a*** memory module ***from a*** host computer in response to a write command or (ii) ***from a*** memory module ***to a*** host computer in response to a read command. *See* Dkt. No. 228 at 32-33 (noting the claims refer to "'caus[ing] the memory module to *receive or output*' a data burst" in response to read or write commands). The Court's construction for "overall CAS latency" does not examine when data is made available

[2] It is undisputed that written description support is required for the "CAS latency" limitation with respect to data being ***written to*** memory modules and data being ***read from*** memory modules under the Court's claim construction. *See generally* Dkt. No. 453 at 1-2, 4.

[redacted]

from a data buffer to a memory device, and Netlist's identification of alleged disclosure for that timing does not create a genuine issue of material fact.

More specifically, Netlist provides the following figure to illustrate [redacted]

[redacted]

Dkt. No. 453 at 5. The figure, however, illustrates the fundamental problem with Netlist's argument—because it illustrates that data is "made available to the memory module" from a host computer at the beginning of [redacted] (when data enters the DIMM connector), and the data is made "available from" the memory module to the host computer [redacted] (when data leaves the DIMM connector). The figure further illustrates that data is made available ***to a data buffer*** from the DIMM connector at a different time [redacted] and data is made available ***from the data buffer*** to the SDRAM memory devices at a different time [redacted] Notably absent from Netlist's argument is any reference to [redacted] much less a comparison between "when a [write] command is executed by the memory module" and the [redacted] time when data is made available to the memory module, as required by the Court's "overall CAS latency" construction.

Netlist's argument that the Court's construction of the CAS latency limitation ends the written description inquiry is wrong. *See* Dkt. No. 453 at 4. Netlist cites to no case law for this incorrect position. To the contrary, a specification can help identify meaning of a claim term without providing adequate written description. *See, e.g., Trading Techs. Int'l, Inc. v. Open E Cry, LLC*, 728 F.3d 1309, 1319 (Fed. Cir. 2013) ("Despite their similarities . . . , claim construction and the written description requirement are separate issues that serve distinct purposes.").

[redacted]

Netlist's argument that Micron failed to move to strike Netlist's expert's opinions is also wrong. Dkt. No. 453 at 6. Micron moved to strike Netlist's expert for not applying the Court's CAS latency claim constructions. *See* Dkt. No. 369 at 9-12.

No genuine issue of material fact exists here. The Court's claim construction is clear, and Netlist has identified no written description for the claims as construed. The Court should grant summary judgment. *See Cisco Sys., Inc. v. Cirrex Sys., LLC*, 856 F.3d 997, 1008 (Fed. Cir. 2017) ("a broad claim is invalid when the entirety of the specification clearly indicates that the invention is of a much narrower scope").

B. There is No Written Description for the "Data Buffer Control Signals" Before the '417 Patent's November 25, 2019 Filing Date

The fundamental dispute between the parties is whether the applications' disclosure of "control signals" in earlier applications provides written description support for the "data buffer control signals" recited in the '417 patent claims.[3] It does not. The '417 patent refers to, and claims, "control signals" and "data buffer control signals" as different claim elements. *See, e.g.,* Dkt. No. 370 at 9. Netlist failed to substantively respond to this argument.

Netlist's only identification of potential written description in earlier applications is the disclosure in U.S. Patent No. 10,489,314 (filed December 28, 2017) of "logic" "providing [first/second] ***control signals*** to the data buffer" and a "circuit 40" "to receive ***control signals*** from the logic element." Dkt. No. 453 at 7-8 (emphases added) (citing '314 patent at Abstract and 7:20-23). In the first instance, the "data buffer" language Netlist cites does not appear in applications earlier than the '314 patent, so at most, if Netlist's argument is adopted, the Court should grant summary judgment that priority is limited to the '314 patent's filing date. The Court, however,

[3] It is undisputed that the term "data buffer control signals" did not appear in the earlier patent applications and was, instead, only added into the '417 patent application. *See generally* Dkt. No. 453 at 6-8.

should not adopt Netlist's argument because the '314 patent's disclosure of logic "control signals" is different than the '417 patent's recital of "data buffer control signals." *See* '417 patent at Abstract ("logic configurable to . . . output registered address and ***control signals and data buffer control signals***"). The '417 patent also claims "control signals" and "data buffer control signals" separately. *See id.* at Claim 1 ("logic . . . configurable . . . to output a set of registered address and control signals . . . wherein the logic is ***further configurable*** to output data buffer control signals") (emphases added). *C.f. Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1368 (Fed. Cir. 2005) (different words presumed to have different meanings or scope).

Netlist's remaining arguments fail to identify any written description in the '417 patent. Netlist's first argument that during prosecution, "the examiner concluded that the 'data buffer control signal' limitation was 'taught by the specification as originally filed'" greatly overstates the examiner's conclusions. Dkt. No. 453 at 7. The examiner was referring to the specification of the '417 patent only "as originally filed" and did not reference the specification of any earlier patent in this family. In any event, the examiner did not point to any support in the specification for the "data buffer control signals" term. *See* Dkt. No. 453-5 at NL-MS-293_00008342-43 (addressing two long claim limitations as the reason for allowance).

Netlist also incorrectly argues that Micron conceded at claim construction that support for "data buffer control signals" is found in the disclosure of "control signals." Dkt. No. 453 at 7 (citing Dkt. No. 143 at 19). First, Netlist cites a claim construction argument made by Samsung, not Micron. *See, e.g.,* Dkt. No. 143 at 19 ("Samsung's construction") and Dkt. No. 160-1 at 17 (identifying the different proposed constructions by Samsung and Micron). Second, the Court rejected Samsung's attempt to base the "data buffer control signals" construction on "the limited disclosure of 'control signals' in the specification." Dkt. No. 228 at 30. Netlist has identified no

[redacted]

reason why the Court should equate these two separate terms now for written description when the Court rejected equating the two terms for claim construction.

The Court likewise should reject Netlist's argument that Micron's expert has taken contradicting positions regarding the limitation. Dkt. No 453 at 7-8. Incorrect. Dr. Stone quoted a "data buffer control signals" teaching in the '417 patent and applied it to a logic diagram. *See* Dkt. No. 453-3 at ¶¶ 254-255. Dr. Stone did not opine that the '417 patent's disclosures of "control signals" provide written description for the claimed "data buffer control signals." Nor did Dr. Stone concede that "the specification discloses control signals for the data buffer," much less the separately claimed data buffer control signals. Dkt. No. 453 at 8. *See* Dkt. No. 453-4 at ¶ 71 [redacted]; *see also* Ex. F (excerpt from 1/11/24 Gillingham Dep. Tr.) at 53:5-10 [redacted]

Netlist's argument that a skilled artisan "would understand" that the data buffer would receive additional control signals is legally flawed. Dkt. No. 453 at 8. "It is not sufficient for purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose." *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997); *see also Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1353-54 (Fed. Cir. 2010). Further, Netlist's reference to "registered CS signals" (Dkt. No. 453 at 8) (*i.e.*, chip-select signals) is flawed because the patent claims expressly identify chip-select signals as the claimed "control signals," not the separately claimed "data buffer control signals." *See* '417 patent claim 1 ("the set of input address and control signals including a plurality of input chip select signals").

[redacted]

No genuine issue of material fact exists here. It is undisputed that the term "data buffer control signals" was added for the first time in the '417 patent specification, and Netlist only relies upon earlier disclosures of a separate claim element "control signals" as alleged support. Summary judgment is appropriate.

IV. CONCLUSION

For the reasons stated above and in Micron's opening brief, Micron respectfully requests that the Court grant its motion for summary judgment that the claims of the '417 patent lack written description.

Dated: February 7, 2024

Respectfully submitted,

/s/ Michael R. Rueckheim

Thomas M. Melsheimer
State Bar No. 13922550
TMelsheimer@winston.com
Natalie Arbaugh
State Bar No. 24033378
NArbaugh@winston.com
WINSTON & STRAWN LLP
2121 N. Pearl Street, Suite 900
Dallas, TX 75201
Telephone: (214) 453-6500
Facsimile: (214) 453-6400

David P Enzminger (*pro hac vice*)
denzminger@winston.com
WINSTON & STRAWN LLP
333 South Grand Avenue, 38th Floor
Los Angeles, CA 90071-1543
Telephone: (213) 615-1700
Facsimile: (213) 615-1750

Michael R. Rueckheim
State Bar No. 24081129
MRueckheim@winston.com
Ryuk Park (*pro hac vice*)
RPark@winston.com
Matthew R. McCullough
MRMcCullough@winston.com
WINSTON & STRAWN LLP

[redacted]

255 Shoreline Drive, Suite 520
Redwood City, CA 94065
Telephone: (650) 858-6500
Facsimile: (650) 858-6559

Matthew Hopkins (*pro hac vice*)
State Bar No. 1500598
mhopkins@winston.com
WINSTON & STRAWN LLP
1901 L Street, N.W.
Washington, D.C. 20036
Telephone: (202) 282-5000
Facsimile: (202) 282-5100

William M. Logan
State Bar No. 24106214
wlogan@winston.com
Juan C. Yaquian (*pro hac vice*)
State Bar No. 24110559
JYaquian@winston.com
WINSTON & STRAWN LLP
800 Capital Street, Suite 2400
Houston, TX 77002
Telephone: (713) 651-2600
Facsimile: (713) 651-2700

Wesley Hill
State Bar No. 24032294
wh@wsfirm.com
Andrea Fair
State Bar No. 24078488
andrea@wsfirm.com
Charles Everingham IV
State Bar No. 00787447
ce@wsfirm.com
WARD, SMITH & HILL, PLLC
1507 Bill Owens Parkway
Longview, TX 75604
Telephone: (903) 757-6400
Facsimile: (903) 757-2323

ATTORNEYS FOR DEFENDANTS MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS, LLC

CERTIFICATE OF SERVICE

I certify that, on February 7, 2024, a copy of the foregoing was served on all counsel of record via the Court's ECF system and email.

/s/ Michael R. Rueckheim
Michael R. Rueckheim

CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this Case.

/s/ Michael R. Rueckheim
Michael R. Rueckheim